**Laboratory Report Cover Sheet**

**18ECE206J ADVANCED DIGITAL SYSTEMS DESIGN**

**Fourth Semester, 2021-22 (Even semester)**

SRM Institute of Science and Technology College of Engineering and Technology

Department of Electronics and Communication Engineering

#### Name :

**Register No. :**

**Day/ Session :**

**Venue :**

**Title of Experiment :**

**Date of Conduction: Date of Submission :**

|  |  |  |
| --- | --- | --- |
| **Particulars** | **Max. Marks** | **Marks**  **Obtained** |
| Pre lab and Post lab | 10 |  |
| Lab Performance | 20 |  |
| Simulation and results | 10 |  |
| Total | 40 |  |

**REPORT VERIFICATION**

**Staff Name : Signature :**

**Aim**

**Design of Shannon’s expansion theorem**

To design and verify the truth table for 6 variable logic function using Shannon

decomposition theorem.

#### Software Requirement

Software : Logisim

#### Theory

One method for obtaining the canonical SOP or POS forms of a logic function for a given

truth table is given by using the Shannon’s Expansion Formulas.

Shannon’s expansion theorem can be used to decompose functions of large numbers of variables into functions of fewer variables. In the previous section, we decomposed a 4-to-1 multiplexer into 2-to-1 multiplexers in order to implement it in a logic block with four- variable function generators. Shannon’s expansion offers a general decomposition technique for any function.

Let us illustrate Shannon’s decomposition for realizing any six-variable function Z(a, b, c, d, e, f). First, expand the function as follows:

Z(a, b, c, d, e, f) = a’. Z(0, b, c, d, e, f) + a . Z(l, b, c, d, e, f)

=a’Z0 + aZ1

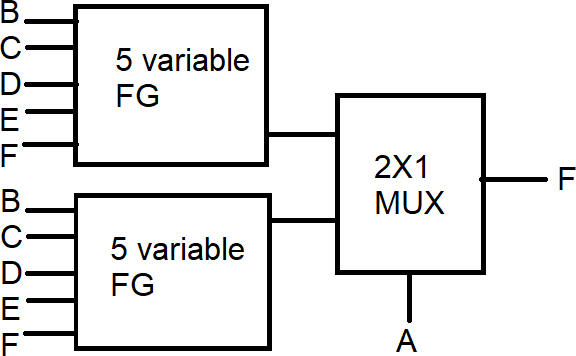
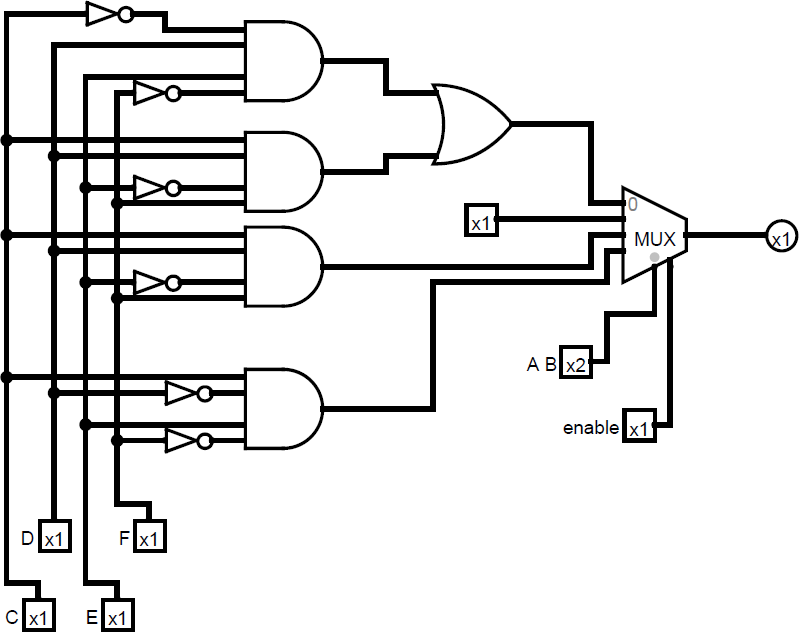


Fig.1 Decomposition of 6 variable function into 5 variable function with 2x1 mux

#### Exercise

* 1. Design the following function using 2x1 mux and 4x1 mux and verify in Logic-sim software

Z= abcd’ef’ + a’b’c’def’ + b’cde’f



**Fig 2. Implementation of 6 variable function using 4x1 mux**

#### Pre lab Questions

1. What is meant by Shannon’s expansion theorem?
2. Implement a Full subtractor using 2x1mux?
3. Implement a Full subtractor using 4x1mux?
4. Implement the given function using 2x1 mux F(A,B,C) = ∑ 1,3,4,6

#### Lab Procedure

1. Decompose the given function by substituting A=0,B=0;A=0,B=1;A=1,B=0; A=1,B=1; and design with 4X1 mux
2. Find the multiplexer in component menu as shown in the fig and select the select line as 2.

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1. Find the gates in the gate menu.
2. Connect with wire just clicking and dragging mouse from one port of the component to other component.
3. Just connect input and output pin, for the select line inputs choose the input data bits as 2.
4. Go to simulate and simulation enabled or Ctrl+E , click on icon , and click oninput pin the value will changed and corresponding output will be updated.

#### Post lab Questions

1. Implement the following expression y=ab+ca’ using 4X1 mux.
2. Design a 16X1 mux only using 2X1mux.
3. Implement a Full adder using 2x1mux?
4. Decompose the given function and implement only using 2x1mux.

F = a’b’c’de + abc’de’ + abc’d’e’ + a’b’c’d’e

**Output :**

#### Result: